REMARKS

Applicant thanks Examiner for the detailed review of the application. The office action refers to the provisional election of claims 1-19 and 43-52 made without traverse in a phone conversation on 3/6/06. Applicant herein affirms the election of claim 1-19 and 43-52 without traverse.

Claim Objections

The Office Action currently objects to applicant's claims 9 and 49-50 due to informalities.

Claim 9 has been amended to depend from claim 8 to provide sufficient antecedent based for "the register." In addition, claims 49-50 have been amended from a storage device to a storage medium to rectify the antecedent basis.

Claim Rejections -35 USC § 102(b)

The Office Action has rejected Claims 1-11, 13-15, 17, and 19, under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,781,187 to Gephardt. (referred to hereinafter as "Gephardt"). Furthermore, The Office Action has rejected Claims 43, 45-46, and 51-52, under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 7,152,169 to Cooper. (referred to hereinafter as "Cooper"). However, the Office Action has failed to make a prima facie case of anticipation for the claims, and such, the applicant respectfully submits that the rejections should be withdrawn.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown in as complete detail as contained in the ... claim." Richardson v., Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Applicant's claim 1 includes the element, "in response to the state of the second processor being active and not in SMI mode (SMM), waiting for the second processor to enter SMM." In contrast, Gephardt only suggest providing commands, such as hold, shutdown, etc., to other processors in SMM through an SMM code/flag value, not indication of a state of a processor. For example, Gephardt discloses at col. 21 the following,

SMM processing unit. Initially, this flag indicates "HOLD" to each slave SMM processing unit. Upon entry of SMM and seeing the HOLD code in that register, each slave SMM processing unit will pause and poll its corresponding SMM code/flag field until it changes. When the master SMM processing unit processes the requested actions for system management (powering down a peripheral, for example), it changes the status of the other processing units SMM code 50 flags with a special command (i.e., note that normally one processing unit cannot affect other processing units channel registers), which will allow them to continue SMM code

As can be seen, the slave **upon entry of SMM** seeing the HOLD code pauses. However, Gephardt only discloses the use of these "commands" once the master and slave processors have entered SMM, not **waiting for** the second processor **to enter SMM** as in applicant's claim 1. Furthermore, Gephardt's disclosure of a code/flag is utilized to request actions for system management through special commands. However, Gephardt never discusses or suggests that the code indicates a state of the processor, such as an "active and not in SMM," as in applicant's claim 1.

Moreover, applicant's claim 43 includes the element, "a storage medium...to hold a system management state of at least the second processor." Cooper suggests that synchronization may be performed at col. 4 lines 49-51 and that "a first logical processor may wait in a loop until it receives a notification from the second logical processor that the second logical processor enters SMM." Therefore, Cooper only suggests a notification from the second processor that it has entered SMM, which may be signal or other notification from the second processor, but never discloses or suggests that a system management state of the second processor is to be held in a storage medium, as in applicant's claim 1.

Therefore, applicant respectfully submits that applicant's claim 1 and 43, as well as their

dependent claims, are now in condition for allowance for at least the reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted, Intel Corporation

Dated: September 20, 2007 /s/David P. McAbee/Reg. No. 58,104/

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